A New Approach to Radio Astronomy Signal Processing:
Packet Switched, FPGA-based, Upgradeable, Modular Hardware and Reusable, Platform-Independent Signal Processing Libraries

Aaron Parsons[1],
Don Backer[1], Chen Chang[4], Daniel Chapman, Henry Chen[2], Pierre Droz[2,4], Christina de Jesus, David MacMahon[3], Andrew Siemion, John Wawrzynek[5], Dan Werthimer[2], Mel Wright[3]

[1] *Astronomy Dept.,*
[2]*Space Sciences Laboratory,*
[3]*Radio Astronomy Laboratory*
[4]*Berkeley Wireless Research Center*
[5]*Dept. of Electrical Engineering and Compute r Sciences*

University of California, Berkeley

ABSTRACT

Our group seeks to revolutionize the development of radio astronomy signal processing instrumentation by designing and demonstrating a scalable, upgradeable, FPGA-based computing platform and software design methodology that targets a range of real-time radio telescope signal processing applications. This project relies on the development of a small number of modular, connectible, upgradeable hardware components and platform-independent signal processing algorithms and libraries which can be reused and scaled as hardware capabilities expand. We have developed such a hardware platform and many of the necessary signal processing libraries for applications in antenna array correlation, wide-band spectroscopy, and pulsar surveys. We present this platform and two applications we have developed for it as demonstrations of the technology. We also identify future directions for the development of this platform, such as packetization, RFI rejection libraries, and real-time imaging.

1. Introduction

Existing radio astronomy instrumentation is highly specialized, with custom, complex, dedicated instruments being built for individual applications. Each instrument takes 3-5 years to design, construct, and debug, and by the time it is deployed, it has usually been made obsolete by the Moore's Law growth of the

electronics industry. This development cycle could be shortened by taking advantage of commodity hardware and developing signal processing libraries which are device independent. There is a growing trend in radio astronomy for high-performance real-time DSP applications such as beam forming, spatial correlation, and wide-band, fine-resolution spectroscopy. The next generation of radio telescopes (eg: Allen Telescope Array (ATA), the Combined Array for Research in Millimeter-wave Astronomy (CARMA), the next generation Epoch of Reionization (EoR) array, and the Square Kilometer Array (SKA)), are being designed and built using large numbers of small antennas. One of the most computationally difficult problems in radio astronomy instrumentation is a real-time imaging system for very large arrays, with computation time scaling as $O(N^2)$. Applications requiring several gigahertz of continuous RF bandwidth over hundreds of physical antennas require peta-operations per second. Such computational requirements are far beyond the capabilities of the general purpose computing clusters which have traditionally been the commodity solution to radio astronomy signal processing. Because of their iteration-based, inherently non-parallel architectures, CPUs can only process a bandwidth equal to their clock rate divided by the number of operations per sample. For computationally intensive applications, this number is low, even for multi-gigahertz processors.

2. FPGAs as Commodity Signal Processing Hardware

Field-Programmable Gate Arrays (FPGAs) are large-scale configurable logic devices with commercial applications that promote commodity pricing. These devices are the keystone technology for developing flexible signal processing hardware. Their reprogrammability and flexibility places them in a middle ground between custom hardware and flexible software: *gateware*. The data-flow processing nature of DSP algorithms matches the stream-based computation model commonly used on FPGAs, with throughput locked to the system clock rate. These elements can provide over 10 times more computing throughput than a DSP-based system with similar power consumption and cost, and over 100 times that of a microprocessor-based system, as a result of the disparity between the inherently sequential execution model of microprocessors and the spatially parallel execution model of a hardware implementation. Furthermore, because of their simple hardware structure, FPGAs scale naturally with each successive generation of silicon processing technology, resulting in the fact that FPGAs are on a faster Moore's Law track than CPUs. Based on current projections for FPGA computing

technology, the SKA computational requirement (on the order of 100 peta-operations per second) will be feasible by 2009, and implementable by 2011, with an estimated cost of $20 million USD per 800 MHz IF channel (Chang et al. 2005).

FPGAs may be the answer for creating DSP hardware with the flexibility to be widely adopted in radio astronomy instrumentation, but Moore's Law growth still dictates that hardware will need to be redesigned every few years. A solution is needed which minimizes the effort of redesign--a solution which minimizes the number of hardware modules which must be redesigned, and abstracts algorithms from hardware so that changing hardware affects only broad-scale implementation choices, not algorithm selection.

3. Hardware Modularity

Hardware modularity requires that a small number of components with consistent interfaces be connectible with an arbitrary number of identical components to meet the computing needs of an application ("computing by the yard"), and that upgrading/revising a component does not change the way in which components are combined in the system. A modular system architecture can provide orders of magnitude reduction in overall cost and design time, and will closely track the early adoption of state-of-the-art IC fabrication by FPGA vendors. The Berkeley Emulation Engine (BEE2) system is one of the first attempts at providing a scalable, modular, economic solution for high-performance radio telescope DSP applications (Chang et al. 2005). Originally designed for high-end reconfigurable computing applications such as DSP and ASIC design, the BEE2 has been conscripted for radio astronomy applications in a collaboration between the Berkeley Wireless Research Center (BWRC), the UC Berkeley Radio Astronomy Laboratory, and the UC Berkeley SETI group.

The BEE2 system consists of three hardware modules developed by graduate students Chen Chang and Pierre Droz of BWRC: the main BEE2 processing board, a high-speed ADC board for data digitization, and an IBOB for high-speed serial communication between the two boards.

The BEE2 board (see Figure 1), intended to be the primary processing engine, integrates 500 Gops/sec of computational power with high-speed I/Os. Its compute power is provided by its 5 Xilinx XC2VP70 Virtex-II Pro FPGAs, each containing 384 18x18-bit multipliers, two PowerPC CPU cores running Linux, and over 74,000 configurable logic cells. In addition, each FPGA can be connected to up to 4 GB of DDR2-SDRAM. External interfaces are available through 10 Gbps ethernet connections, as well as 100 Mbps ethernet and RS232 serial ports.

IBOB (Internet BreakOut Board, see Figure 2) boards are primarily responsible for packetizing ADC data onto the ethernet protocol. Each board provides two connectors for I/O card attachment, and two 10 Gbps ethernet connectors for interfacing to BEE2 boards. Data packetization and serialization is performed by a Xilinx XC2VP50 FPGA which provides 232 18x18-bit multipliers, two PowerPC CPU cores, and over 53,000 logic cells. This FPGA, along with 36 Mbit of on-board ZBT SRAM, allows the IBOB to perform a significant amount of data preprocessing before handing off to the BEE2.

An ADC board (see Figure 3) was designed to mate directly to an IBOB board for high-speed serial data I/O. Analog data is digitized using an Atmel AT84AD001B dual 8-bit 1 Gsample/sec ADC chip, and can digitize two streams at 1 Gsample/sec or a single stream at 2 Gsample/sec. This board may be driven with either single-ended or differential inputs.

Communication between hardware modules takes place over standard 10 Gbit ethernet protocol, allowing for the eventual integration of commercial switches and processors. Any of these boards may be upgraded separately to use the latest FPGA chips, and all of them may be upgraded together to take advantage of advancements in inter-board communication. These three boards may be combined to provide ample computational resources for any radio astronomy application: spectral analysis, antenna correlation, band extraction, and back-end analysis. This modular hardware platform provides astronomers with the ability to connect as many boards as necessary to meet the needs of their application.

4. Gateware Reusability

The advantages of a flexible, upgradeable hardware architecture for radio astronomy signal processing cannot be realized without a set of reusable libraries for quickly implementing signal processing algorithms in FPGAs. These libraries and their underlying algorithms must be abstracted from the hardware involved in order to support changes and upgrades in hardware technology, and to be of independent use to the reconfigurable computing community. The viability of developing such libraries has been already demonstrated: several of the original libraries we developed were targeted for the SERENDIP V board we designed as a first implementation of a multipurpose, FPGA-based signal processing engine for radio astronomy (http://seti.berkeley.edu/casper). This board and associated libraries have proven useful in several applications at Arecibo (Heiles et al., 2005, http://seti.berkeley.edu/galfa), Nancay (Backer et al., 2005), for prototype antenna arrays (Backer and Bradley, 2005), and others. Most importantly, the libraries developed for these applications, which include designs for Polyphase Filter Banks (PFBs), Fast Fourier Transforms (FFTs), accumulators, digital mixers, digital oscillators, quadrature baseband down-converters, and FIR filters, were able to be ported to the new BEE2 architecture without modification.

An important tool which has helped make it possible to write reusable gateware libraries is the Xilinx System Generator package for the Mathworks Simulink language. Much as a C compiler translates platform-invariant ASCII code into processor-specific byte-code, Simulink translates designs written using a standard set of FPGA components into chip-specific VHDL or Verilog that is synthesized into a final chip configuration. Using Simulink and Xilinx System Generator, we abstract the physical FPGA fabric into a set of parameterizable library blocks for implementing signal processing algorithms, and for interfacing with abstracted hardware-specific components such as ADCs, DRAM, and other FPGAs.

In order for the signal processing algorithms we develop to be useful in a variety of applications, it is important that they be parameterized such that they be customizable for size, behavior, and speed. This requirement adds complexity to the initial design of these libraries, but dramatically enhances their applicability and potential for longevity as hardware evolves; it is important that algorithms be expandable to take advantage of the inevitable increase in chip resources. This design principle has an added feature that it decreases the time

necessary for testing by allowing one to debug scale models of systems which are behaviorally identical to the larger systems and are derived from the same parameterization code. This feature has been invaluable in speeding the deployment of our various demonstrator projects.

5. DSP Libraries

We have found it useful and convenient to establish a general architectural consistency between the gateware libraries we have designed. Firstly, all modules operate on a vector-warning architecture whereby a single bit signal is passed along with a data stream, and is active the clock-cycle before the first valid data appears on that stream. This enables library components to phase themselves correctly to the data stream, and removes any effect pipeline delays might have on downstream modules, effectively allowing modules to be swapped in to and out of designs without affecting other modules. Secondly, data samples are interpreted as 2's compliment, fixed-point numbers in the range [-1,1). Modules which enable the magnitude of samples to grow (such as the FFT), have selectable down-shifting or overflow detection to prevent bit growth. In addition to libraries implementing digital mixers, oscillators, baseband down-converters, decimating FIR filters, matrix transpositions, and accumulators, we have written three libraries which will be instrumental in implementing the next generation of spectrometers and correlators.

5.1. The FFT Library

The first parameterized library we developed under Simulink was for an FFT more efficient than those commercially available in order to gain higher spectral resolution for a SETI spectrometer. To do this, we implemented a radix-2 biplex pipelined FFT (Rabiner and Gold, 1975, see Figure 4) capable of analyzing two independent, complex data streams or four real data streams simultaneously using one quarter the FPGA resources of commercial designs (Dick, 2000). Besides its increased efficiency, this design is superior in its ability to analyze the full input bandwidth at the quiescent clock rate without need of a period of off-line computation during which input samples are not accepted. Instead, this fully pipelined architecture operates at the full clock rate from stage to stage without needing extra buffering. Additional features which we have

developed for this library are modules which use in-place buffering to unscramble the standard bit-reversed output order of the spectral data, and modules for extracting two real FFTs from a single complex FFT using Hermitian conjugation and interpolation. Although this library was developed primarily to be coupled with the Polyphase Filter Bank (PFB) library we discuss next, it has been used in stand-alone applications for fine-resolution spectroscopy applications such as the 128 million channel SETI spectrometer discussed in the next section of this paper.

5.2. The Polyphase Filter Bank Library

The PFB (see Figure 5) is an efficient implementation of a digital filter bank which decomposes a set of decimating FIR filters into a single convolution followed by a Fourier transform (Crochiere and Rabiner, 1983, and Vaidyanathan, 1990, see Figure 6). Since the Fourier transform has already been highly optimized algorithmically, this results in an extremely efficient implementation. Alternately, the PFB may be regarded as an improvement on the FFT which uses additional hardware in the form of a phased FIR front-end filter to improve the filter response of each spectral sample in the FFT (see Figure 7). Using selectable, parameterized windowing functions, our design allows for the adjustment of the out-of-band rejection, passband ripple/rolloff, and absolute width of each filter. Because of its near-ideal filter shapes, our PFB library has already seen widespread use in the radio astronomy community in applications such as 21 cm hydrogen surveys (Heiles et al., 2005), pulsar surveys (Backer et al., 2005), antenna arrays (Backer and Bradley, 2005), VLBI, and others.

5.3. The X Engine Library

We are in the process of testing a new library for applications in the exploding field of antenna array correlation. With the quantity of new arrays under development, the need for current/future correlators is tremendous. As discussed previously, the trend in these arrays is toward large numbers of antennas, requiring careful attention to the scalability of designs. In collaboration with Lynn Urry of UC Berkeley's Radio Astronomy Lab, we have developed and implemented a parameterized module for computing and accumulating baselines in an FX correlation architecture (see Figure 8).

In this correlator architecture, spectral data for each antenna is computed using our PFB design, and each of our "X Engine" modules is responsible for handling all of the baseline data for a single frequency. These dedicated-frequency modules have an advantage over dedicated-baseline modules in that the it requires only same number of modules as antennas (each module can handle 1/N spectral channels), and each module may be split across multiple FPGAs, as indicated in the Figure 8. This architecture allows maximum scalability by dividing computational resources along both axes of the NxN matrix of calculations to be performed (see Figure 9). This enables the correlation of any number of antennas and frequency channels to be mapped into modules containing any sized FPGA. This architecture also has the feature of attaining perfect hardware efficiency by multiplexing data through multipliers.

6. Demonstration Projects

We have collaborated in two UC Berkeley projects which may serve as demonstrators of the applicability of our modular approach to radio astronomy signal processing.

6.1. A 128 Million Channel SETI Spectrometer

The first of these is a SETI spectrometer for use by NASA's Jet Propulsion Laboratory. This application required the analysis of a selectable 200 MHz band at under 2 Hz resolution for anomalous narrow-band emission. This 128 Million channel spectrometer was implemented on an IBOB module connected to one BEE2 module (see Figure 10).

Although the requirements of this application did not tax the computational resources of these two boards, it was nonetheless an important demonstrator of the design-flow and hardware connectivity which are instrumental to the rapid development of applications on our modular hardware. In the development of this spectrometer, every hardware component and interface on every board, with the exception of the ZBT SRAM on the IBOB, was tested. The reusability of the FFT and PFB libraries, which were originally developed for the

SERENDIP V architecture, was also demonstrated. This instrument is currently in operation at NASA's Goldstone Deep Space Communications Complex.

6.2. A 32 station FX Correlator

Our second demonstrator project is a 32 station, full Stokes, FX correlator for a new dipole antenna array being developed by UC Berkeley's Don Backer and NRAO's Rich Bradley (Backer and Bradley, 2005) for probing the period of early structure formation in our universe--the Epoch of Reionization (EoR). Our prototype imager demonstrates innovative and crucial technologies needed for the next generation of radio telescopes such as the ATA, CARMA, the SKA, and the next generation EoR array.

The first phase of development (see Figure 11) was to implement an 8 antenna correlator on 4 IBOBs and 1 BEE2 which bypassed the need for inter-IBOB spectrum synchronization by using IBOB compute resources only for digital band extraction (mixing, filtering, and decimation). PFB spectral decomposition for the antennas was moved into four FPGAs on the BEE2, and correlation was performed in the fifth. In this phase, the number of spectral channels was limited to 1024 as a result of the chip resources required for performing the N_{freq} x 128 dual-antenna, complex sample matrix transpose necessary for the correlation X Engine to meet the bandwidth requirements into DRAM.

Our next step (see Figure 12) will be to provide for the synchronization of spectra between IBOBs, so that the PFB and following matrix transpose can be moved into the IBOB's FPGA and ZBT SRAM, respectively. Once this has been achieved, we will be able to attain up to 8096 spectral channels, and the recovered BEE2 compute resources will allow us to correlate a maximum of 32 antennas before we require another BEE2 module to meet the bandwidth requirements between the IBOB's PFB and the BEE2's X Engines. After 32 antennas, our next step will be to develop a fully packetized, switched correlator to provide for the interconnect between the IBOBs and multiple BEE2s.

7. Conclusions

The building blocks for the modular architecture we propose for the future of radio signal processing have already proven themselves in several applications. However, a couple of key technologies remain to be developed before the full potential of this architecture can be realized. A major problem in the design of large N array systems has been the routing of high-bandwidth spectral data. Each cross-correlation element must receive data from every antenna's spectrometer, and many processors are needed to handle the aggregate data rate. This leads to an unmanageable (~200,000) number of high-speed interconnections. The correlator connection problem can be solved by packetizing each antenna's spectral data and routing data through commercial off-the-shelf network switches to an array of FPGA-based cross-correlation elements. This packetization scheme remains to be developed.

In addition, more complex, algorithmically experimental libraries need to be developed to harness the promise of digital solutions to RFI and other limiting factors in telescope sensitivity such as ionospheric turbulence. FPGAs can be programmed to remove known RFI by notching interfering signals in the time and frequency domains, then computing the inverse FFT and outputting the time-domain data. In radio interferometric arrays, the phase across the wavefront can be digitally adjusted to correct for atmospheric turbulence or RFI, providing "digital adaptive optics" by dynamically fitting for distortion. These and other yet-to-be-determined algorithms and libraries must be developed for scientific-grade astronomy computing.

However, we have demonstrated the applicability of our high-performance computing platform and tools to current and future instruments in antenna array correlation, spectroscopy, pulsar surveys, and SETI—a platform which, with its modular architecture and industry standard protocols, will allow astronomers to quickly upgrade performance as the speed of commercially available switches and FPGAs increases.

8. Acknowledgments

The BEE2, IBOB and ADC boards were developed by graduate students Chen Chang and Pierre Droz of the Berkeley Wireless Research Center with the guidance of John Wawrzynek, Bob Brodersen, and Dan Werthimer. We would like to thank Chen and Pierre for their continued work on device drivers and tool-flow which has promoted rapid development for the BEE2 system. We thank Henry Chen for his contributions in hardware testing, tool development, and design management, and students Andrew Siemion, and Daniel Chapman for their work in writing server code and plotting tools for backend analysis in spectrometer and correlator applications. We would also like to recognize Lynn Urry for his contributions to the algorithms used in the X Engine, and thank David MacMahon for his advice on correlator architectures. The FPGA and ADC chips were generously donated by Xilinx and Atmel, respectively. This research was supported by grants from NASA and the National Science Foundation.

9. References

Backer, D. and Bradley, R., *NRAO newsletter*, no. 102, pp. 27, January 2005.

Backer, D., Demorest, P., Ramachandran, R., Stairs, I., Ferdman, R., Nice, D., Cognard, I., "Realtime Astronomy Signal Processing in PC Clusters," *URSI GA*, Proc. XXVIII, India, COM9-01696, October, 2005.

Chang, C., Wawrzynek, J., Brodersen, R.W. "BEE2: A High-End Reconfigurable Computing System," *IEEE Design and Test of Computers*, vol. 22, no. 2, pp. 114-125, March/April 2005.

Crochiere, R.E., and Rabiner, L.R., "Multirate Digital Signal Processing," Englewood Cliffs, NJ: Prentice Hall, 1983.

Dick, C., "High-Performance 1024-Point Complex FFT/IFFT V2.0," *Xilinx Application Note*, 2000 (see http://www.xilinx.com).

Heiles, C., Goldston, J., Mock, J., Parsons, A., Stanimirovic, S. "GALFA Hardware and Calibration Techniques," *AAS*. vol. 2004AAS, no. 2005.7807H, December 2005.

Rabiner, L. R. and Gold, B., *Theory and Application of Digital Signal Processing*, Prentice-Hall Inc., 1975.

Vaidyanathan, P.P., "Multirate Digital Filters, Filter Banks, Polyphase Networks, and Applications," *Proc. IEEE*, vol. 78, pp. 56-93, January 1990.

Werthimer, D., Ng, D., Bowyer, S., Donnelly, C., "The Berkeley SETI Program: SERENDIP III and IV

Instrumentation," in "Progress in the Search for Extraterrestrial Life," ed. S. Shostak, (Astron. Soc. Pac.

Conf. Ser.), 1995.

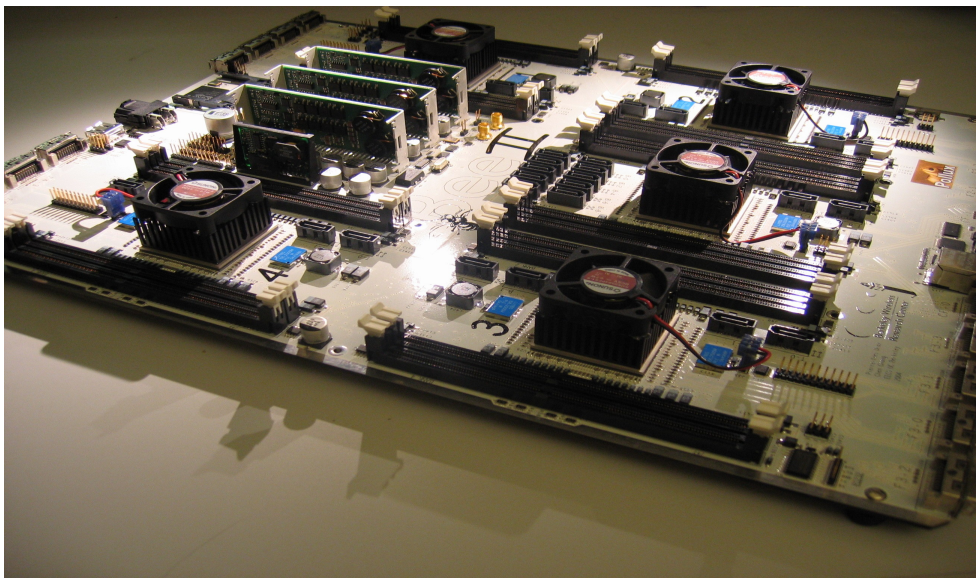

Fig. 1. Each BEE2 processor board can compute at 500 Gops/sec and has 180 Gbits/sec of I/O. Each board has five FPGA's in a star network, 40 GBytes RAM and eighteen 10 Gbit ethernet ports. The boards can be connected together like a Beowolf cluster: 40 boards fit into a rack, and yield about 20 Teraops/sec.

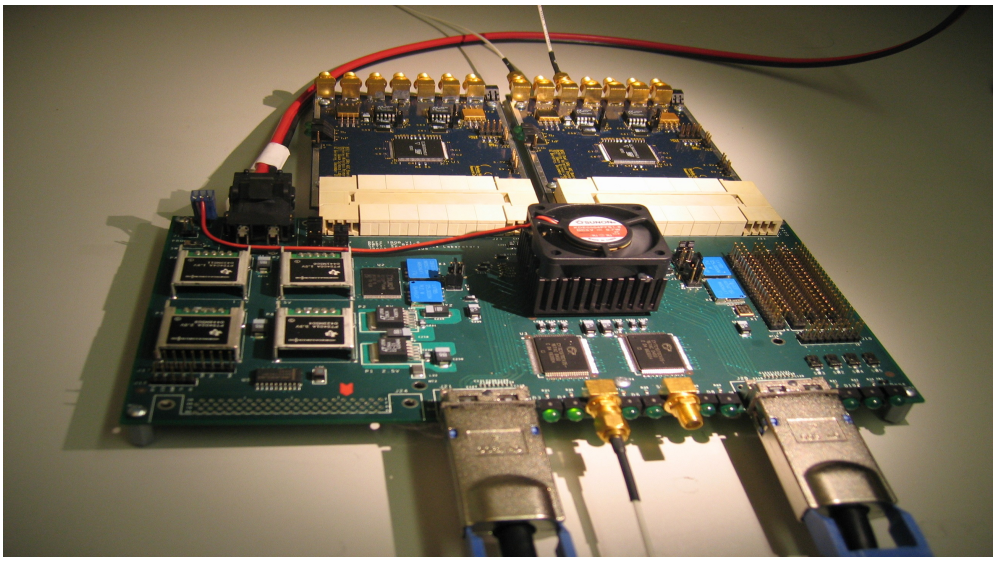

Fig. 2. The IBOB contains a single FPGA and ZBT SRAM for data preprocessing and packetization into the 10 Gbit ethernet format.

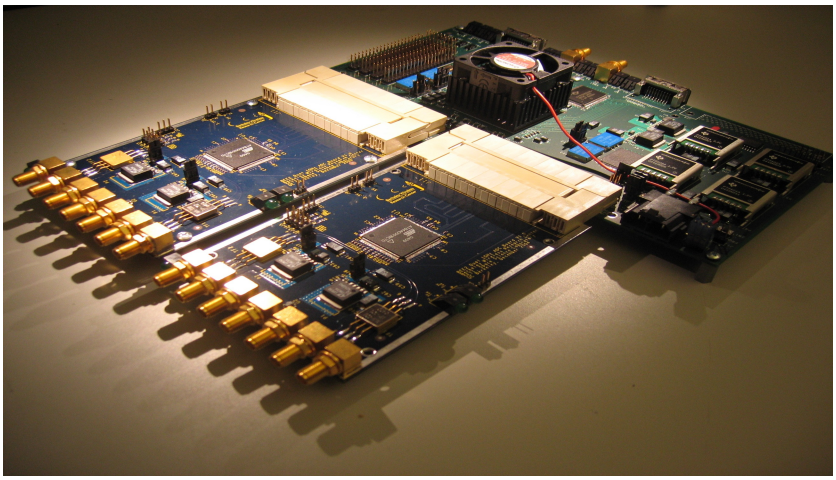

Fig. 3. The ADC Board mates directly with the IBOB and can digitize a single stream at up to 2 Gsamples/sec, or two streams at 1 Gsample/sec.

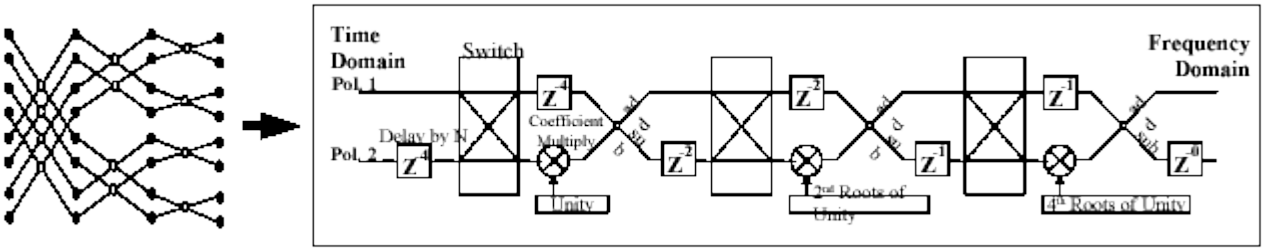

Fig. 4. The Biplex Piplined FFT architecture reuses butterfly computations for streaming applications. This architecture is capable of performing two complex FFTs simultaneously.

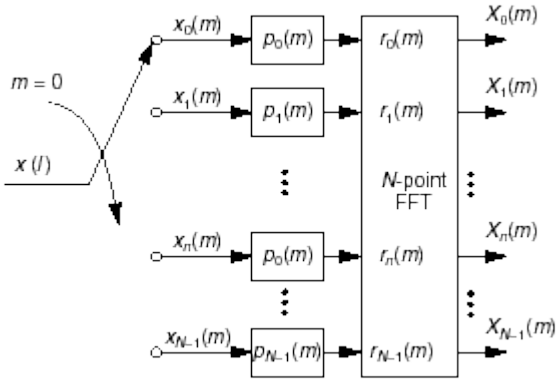

Fig. 5. The Polyphase Filter Bank (PFB) is mathematically equivalent to a bank of FIR filters, but takes advantage of the highly optimized FFT algorithm for computational efficiency.

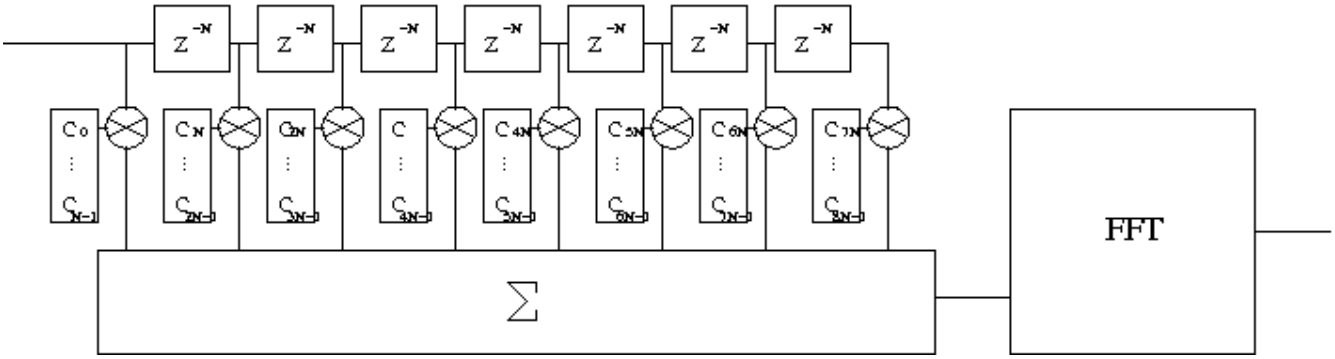

Fig. 6. Our implementation of the PFB uses a phased FIR filter with coefficients derived from sin(x)/x times a windowing function. This diagram illustrates an 8-tap filter.

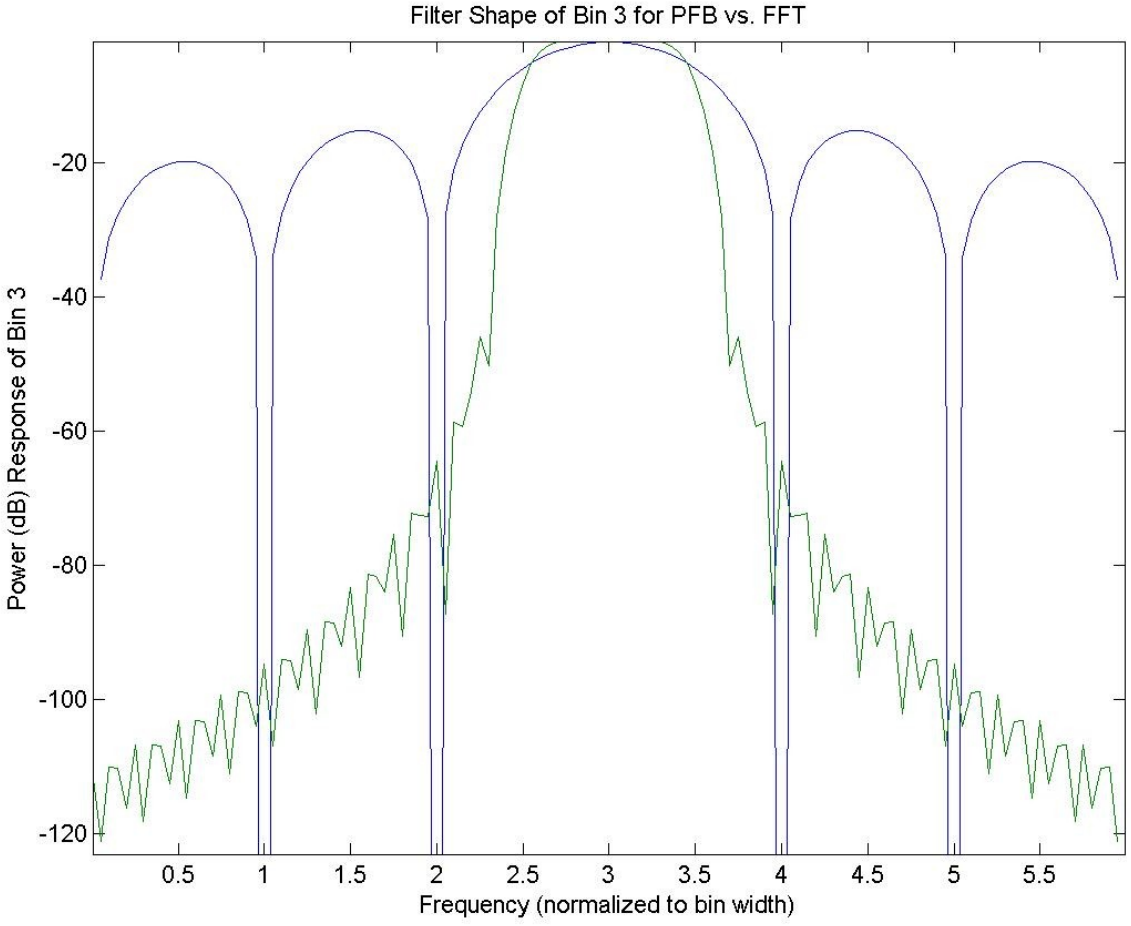

Fig. 7. The PFB provides better out-of-band rejection than an FFT. Graphed here is the channel response of an 8-tap, hamming-windowed PFB (green) vs. an FFT (blue).

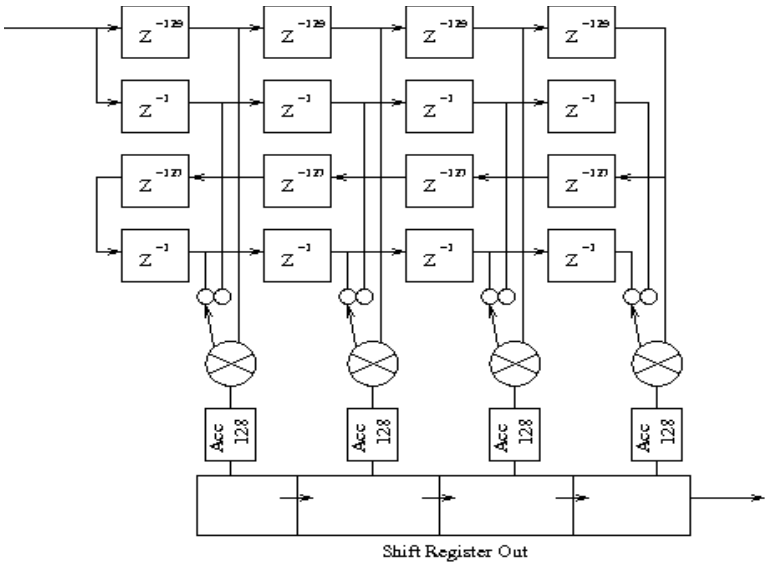

Fig. 8. Our implementation of an X Engine correlator delays antenna streams to match the baselines which are to be cross-multiplied. Multipliers are multiplexed between different baselines to avoid invalid computations and thus attain 100% multiplier efficiency. This design has the feature that it may be divided across chips or boards between any stage.

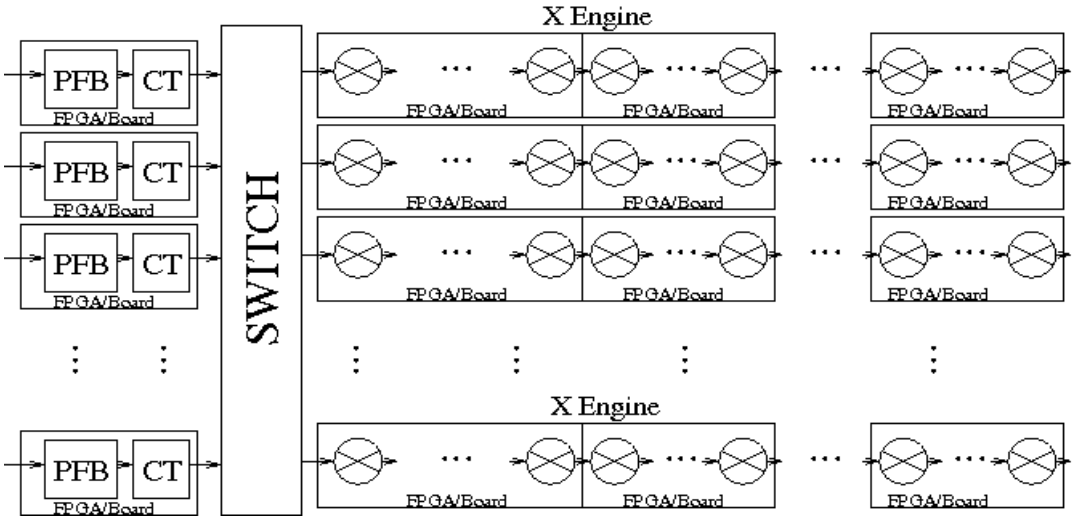

Fig. 9. Applying our X Engine architecture to a general FX correlator, we see how an arbitrarily large correlation may be mapped into multiple hardware modules.

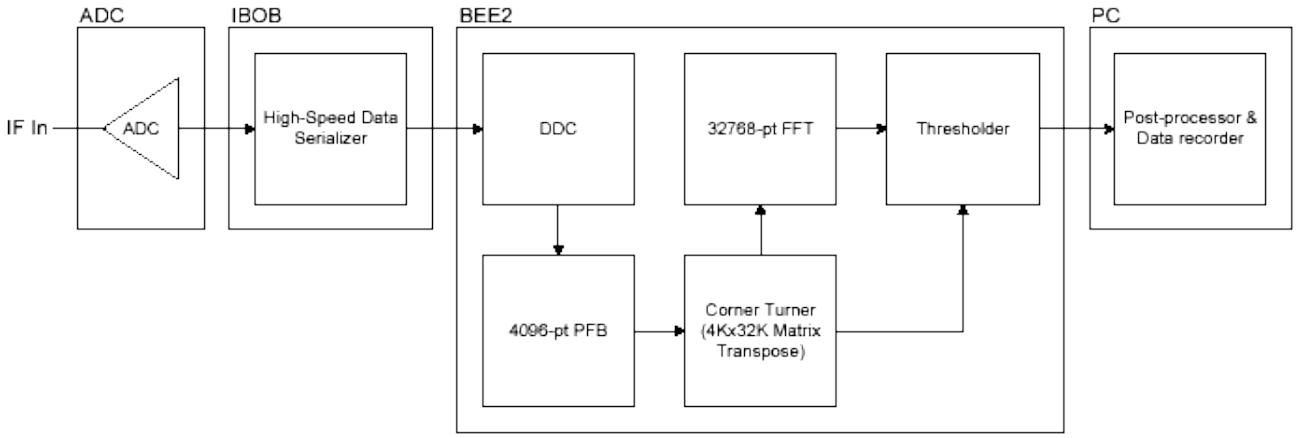

Fig. 10. The 128 Million Channel SETI Spectrometer was implemented on one IBOB and one BEE2 module. Undertaxing computer resources allowed us to split the Digital Down-Converter (DDC), PFB, matrix transpose (Corner Turner), FFT, and Thresholding/Detection into separate FPGAs.

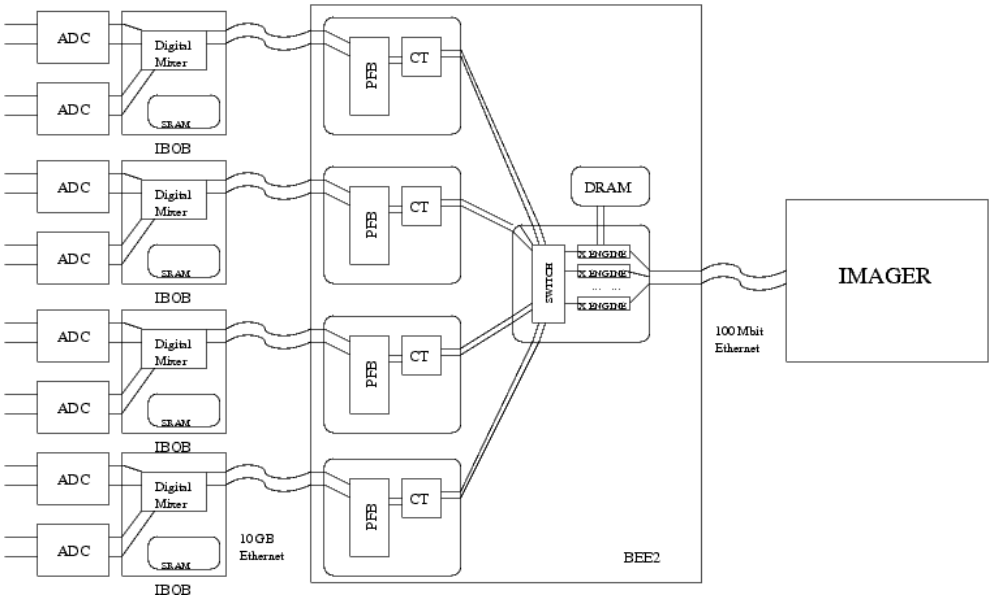

Fig. 11. The 8-station correlator was implemented with four IBOBs and one BEE2 module. In this first phase of correlator development, the problem of synchronizing spectra on multiple IBOBs was avoided by performing the spectral decomposition of all antennas on the BEE2.

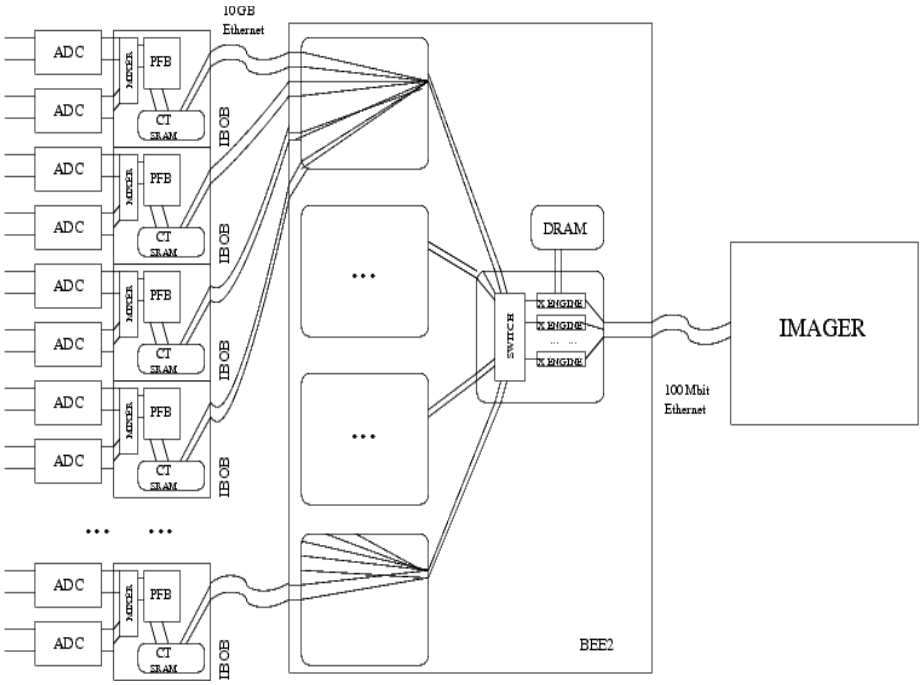

Fig. 12. The upcoming 32 station correlator requires the synchronization of spectra across IBOB boards, but allows for the expansion of the number of antennas and frequencies by moving the spectral decomposition and matrix transpose into the IBOB. The next step in number of antennas requires us to fully develop data packetization to allow the splicing of a commercial switch between the IBOBs and the BEE2s.